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John Stattler

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Steven Teig, et al.

Serial No.: Not Yet Assigned

Filed: Herewith

For: **Simulating Diagonal Wiring Directions Using Manhattan Directional Wires (As Amended)**

PRELIMINARY AMENDMENT

Box PATENT APPLICATION
Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

This Preliminary Amendments is concurrently filed with the above-entitled application, which is a continuation application of a presently pending application Ser. No. 09/681,776, entitled "Diagonal Wiring Architecture For Integrated Circuit", filed on June 3, 2001, which is a continuation application of a presently pending application Ser. No. 09/733,104, entitled "Multi-Directional Wiring On A Single Metal Layer," filed on

December 7, 2000. **Applicants respectfully request that claims 1-35 be canceled (pursuant to the amendment below) before calculation of the filing fee.**

IN THE TITLE

Please replace the current title, " Diagonal Wiring Architecture For Integrated Circuit" with "Simulating Diagonal Wiring Directions Using Manhattan Directional Wires."

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation application of United States Patent Application Ser. No. 09/681,776, entitled "Diagonal Wiring Architecture For Integrated Circuit", filed on June 3, 2001, which is a continuation application of United States Patent Application Serial No. 09/733,104, entitled "Multi-Directional Wiring On A Single Metal Layer", filed on December 7, 2000.

IN THE SPECIFICATION

Please delete paragraphs [0004], [0005], and [0006].

SUMMARY OF THE INVENTION

Diagonal wiring directions in integrated circuits are simulated with wires deposed in purely Manhattan directions (e.g., horizontal and vertical directions). A metal layer of an integrated circuit contains at least two pairs of conductors to interconnect one or more points on the integrated circuit. As used herein, a conductor comprises one or more wires, and a wire comprises a continuous segment deposed in a single direction. Each pair of conductors, used to simulate the wiring direction, includes two wires. The first wire, which has a first wire length with first and second ends, is deposed in a first Manhattan direction relative to the boundaries of the integrated circuit. The second wire, which has a second wire length with first and second ends, is deposed in a second Manhattan direction, and is coupled to the second end of the first wire. The first Manhattan direction is different than the second Manhattan direction. The effective wiring direction of the pairs of conductors comprises an angle, A, measured relative to the boundaries of the integrated circuit. Specifically, the effective wiring direction is defined by the expression Tan A = Y/X, wherein, Y defines a line segment with a distance that starts from the second end of the second wire in the last conductor pair and ends at an intersection with a line segment propagated from the first end of the first wire and in the direction of the first wire, and X comprises a distance, measured in the direction of the first wire, that starts from the first end of the first wire and ends with the intersection of the Y line segment.

The first Manhattan direction includes either a horizontal or vertical direction, and the second Manhattan direction includes either a horizontal or vertical direction, opposite from the first Manhattan direction. In one embodiment, the Manhattan directional wires are configured to simulate a 45 degree wiring direction, and, in another embodiment, the Manhattan directional wires are configured to simulate a 60 degree wiring direction. The pairs of conductors may be configured, essentially in parallel, to generate tracks of conductor on a metal layer in the simulated direction.

IN THE CLAIMS

Please cancel claims 1-35.

REMARKS

This Preliminary Amendments is concurrently filed with the above-entitled application, which is a continuation application of a presently pending application Ser. No. 09/681,776, entitled "Diagonal Wiring Architecture For Integrated Circuit", filed on June 3, 2001, which is a continuation application of a presently pending application Ser. No. 09/733,104, entitled "Multi-Directional Wiring On A Single Metal Layer " filed on December 7, 2000. In this Preliminary Amendment, Applicants have changed the title of this application, inserted a reference to the related parent application, deleted paragraphs in the Summary of the Invention, and canceled claims 1-35. Accordingly, claims 36-47 are currently pending in this application.

Respectfully submitted,

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Dated: January 11, 2002

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